CLAIMS

1. (Currently Amended) A system for transferring data from an incoming source to an outgoing destination, the system comprising:

a buffer storage coupled to the incoming source for receiving and storing telephony data from the incoming source wherein the incoming data is organized into timeslots, wherein the buffer storage is organized so each timeslot corresponds to a unique word location in the buffer storage;

a buffer storage address generator for sequentially addressing the buffer storage so that incoming data is stored sequentially within the buffer storage;

address storage including one or more addresses for accessing the buffer storage;

an address storage generator for sequentially accessing the one or more addresses stored in the address storage;

a clock having a clock cycle and outputting a clock signal;

wherein the buffer storage and address storage address generators are coupled to a signal derived from the clock signal so that a word of data is stored into the buffer storage at the start of each clock cycle and a word of data is read out from the buffer storage by the end of each clock cycle; and

an output stage, wherein the output stage retrieves data from the buffer storage in accordance with the one or more addresses accessed by the address generator.

2-4. (Cancelled).

5. (Previously Presented) The system of claim 1, wherein a word location in the buffer storage is 32 bits in length, wherein the addresses include bits, wherein the lower-order

two bits of each address are used to identify one of four bytes in a word location in the buffer storage.

6. (Cancelled)

7. (Previously Presented) The system of claim 5, wherein four consecutive addresses stored in the address storage are used to each identify a portion of data from one or more locations in the buffer storage.

8. (Currently Amended) A hardware switching system for routing digital data streams in a network, the hardware switching system including;

a memory for storing incoming telephony data organized into timeslots;

an indirect memory addressing mechanism for accessing incoming data stored in the memory including means for generating addresses for storing the incoming data into the memory, the means including a clocked counter for increments of plurality of bytes, wherein on each clock signal, data is read into and read from buffer storage; and

an output control coupled to the indirect memory addressing mechanism for selectively outputting portions of the data in accordance with the indirect memory addressing mechanism.

9. (Previously Presented) A method for switching digital data streams in a network, wherein the digital data streams include timeslots, the method comprising:

storing the incoming data in a memory in accordance with the timeslots; and

indirectly accessing the memory to determine which portions of the data to output; wherein the incoming and output data is telephony data organised into multiple timeslots, the method further comprising:

the step of storing incoming data in a memory including the substep of assigning memory locations to timeslots so that incoming data in a predetermined timeslot is stored in a predetermined memory location; and

the step of indirectly accessing the memory further comprising the substeps of:

using multiple addresses to access multiple memory locations wherein only a portion of each memory location is used; and

combining the data in the accessed multiple memory locations to form output data to be assigned to a single timeslot.

10. (Cancelled)

11. (Original) The method of claim 9 stored in a machine-readable medium.

12. (Previously Presented) The system of claim 1, wherein a number of outgoing timeslots differs from a number of incoming timeslots.

13. (Previously Presented) The system of claim 12, wherein the transfer of data from the incoming source to the buffer storage is not synchronized with the transfer of data from the buffer storage to the output stage.

14. (Previously Presented) The system of claim 1, wherein the transfer of data from the incoming source to the buffer storage is synchronized with the transfer of data from the buffer storage to the output stage.

15. (Previously Presented) The method of claim 9, wherein a number of outgoing timeslots differs from a number of incoming timeslots.

16. (Previously Presented) The method of claim 15, wherein the transfer of data from the incoming source to the buffer storage is not synchronized with the transfer of data from the buffer storage to the output stage.

17. (Previously Presented) The method of claim 9, wherein the transfer of data from the incoming source to the buffer storage is synchronized with the transfer of data from the buffer storage to the output stage.

18. (Previously Presented) The system of claim 8, wherein the address generating means uses a hashing function to map timeslots to arbitrary locations.

19. (Previously Presented) The system of claim 1, wherein the transfer of data from the incoming source to the buffer storage is not synchronized with the transfer of data from the buffer storage to the output stage.

20. (Previously Presented) The method of claim 9, wherein the transfer of data from the incoming source to the buffer storage is not synchronized with the transfer of data from the buffer storage to the output stage.

21. (New) The system of claim 1, further comprising a counter for receiving the clock signal and incrementing sequentially a plurality of bytes.